REMARKS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-17 are currently under consideration. Claims 18-26 have been withdrawn from consideration. The Examiner is respectfully requested to reconsider his rejections in view of the amendments and remarks as set forth below.

Rejection Under 35 USC §102

Claims 1, 13, 14, 16, and 17 stand rejected under 35 USC §102(e) as being anticipated by Jun et al. (USP 6,406,948 B1). This rejection is respectfully traversed.

The Examiner again points out that Jun et al. shows in Figure 10 pairs of diodes which appear to be stacked. The Examiner also states that during normal operation the diodes are reversed-biased and when an ESD event occurs the diodes are forward-biased to conduct the ESD current. In the Examiner's response to Applicants' arguments, the Examiner points out that the prior art includes all parts of a patent including the drawings. However, Applicants still disagree with the Examiner's understanding of the teaching of Jun et al.

First, Applicants wish to point out that there is an exception to the rule that one section of the patent does preclude another section from being reasonably relied upon. That is, the case when there is an obvious error, the error cannot be relied upon. In

particular, MPEP §716.07, and the case of In Re Yale quoted therein indicates that when there is an error that would have been obvious to one of ordinary skill in the art that the erroneous material is not put in the possession of the public. Applicants submit that this is the case in the present situation.

That is, the disclosure includes almost no description of Figure 10 except to indicate that it relates to the schematic of Figure 9. The schematic of Figure 9 indicates that there is no stacked diode, but rather, large area diodes. Applicants submit that the meaning of Figure 10 of the two connected diodes is not that these are stacked diodes, but rather that these indicate the larger sized diodes. Applicants submit that this is the correct interpretation since Figure 9 is consistent with the remaining specification, while Figure 10 appears to be contrary to the teachings of the specification. Thus Applicants submit that it would be clear to one having ordinary skill in the art that the Jun et al. reference does not intend to teach stacked diodes. Accordingly, Applicants submit that this reference does not teach the feature of stacked diodes as suggested by the Examiner.

Further, it is noted that claim 1 also describes that the diodes are reversed-biased and when an ESD event occurs, the diodes are forward-biased. The Examiner states that this is disclosed in Jun et al., however, Applicants do not see any description of this

feature in the reference. The Examiner is requested to point out where in the specification this feature is found. For these reasons, Applicants submit that claim 1 is allowable.

In regard to claim 13, the Examiner states that the reference shows a PN junction formed between a first source/drain and the substrate of an MOS. However, Applicants submit that element 14 is not a source or drain of the MOS. Instead, the source/drain regions are described as element 32 at column 3, line 28. Accordingly, Applicants submit that this claim is additionally allowable.

In regard to claim 14, the Examiner indicates that one skilled in the art would recognize that gate electrodes must be connected to power lines as a necessary condition for the device to work. Applicants disagree.

First, Applicants submit that since the Examiner must rely on the skill of one in the art, that this should be an obviousness rejection rather than an anticipation rejection. Further, it certainly would be possible for a different terminal, such as a source terminal to be connected to the power line and the gate to be connected to some other triggering mechanism. Since the Jun et al. reference does not point out that the gate electrode is connected to the power line, there is no reason for one having ordinary skill in the art to assume that it would.

Since claims 16 and 17 depend from allowable claim 13, these claims are also considered to be allowable.

Rejection Under 35 USC §103

Claims 2-4 stand rejected under 35 USC §103 as being obvious over Jun et al. In regard to claim 2, the Examiner states that the reference is formed by placing a doped area of a first conductivity type in a first well of a second conductivity type and where the deep well of the first conductivity type is formed under the first well to isolate the first well from a substrate of the second conductivity type. The Examiner admits that the reference does not show a doped area in the first well, but that it would have been obvious to insert such a region.

Applicants disagree that it would be obvious to insert such a region since there is no hint of doing so in the reference and no motivation for doing so. In regard to claim 3, Applicants submit that region 16 is not a well as suggested by the Examiner and accordingly the Examiner's reading on region 16 as being surrounded by well 12 is not appropriate. Accordingly, Applicants submit that claim 3 is additionally allowable. In regard to claim 4, this claim depends from claim 2 and as such is also considered to be allowable.

The Examiner rejected claims 5-12, and 15 as being obvious over Jun et al. and further in view of Watt (USP 5,623,156). This rejection is respectfully traversed.

In regard to claim 5, the Examiner points out that Watt shows an ESD clamp circuit 24. The Examiner submits that it would have been obvious to use such a claim circuit in the device of June et al. However, Applicants wish to point out that claim 5 also states that the clamp circuit is set between a first power line and a second power line. In Watt, there are two ESD clamps, 24 and 26 and these do not extend between the power supply buses V_{ssi} and V_{ddi}. Accordingly, Applicants submit that claim 5 is additionally allowable.

In regard to claim 6, the claim states that the two source/drains are coupled to the first and the second power line. As discussed above, the source and drain are not connected to V_{ssi} and V_{ddi}. Instead they are connected to V_{ssi} and V_{sso}. Accordingly, Applicants submit that claim 6 is likewise additionally allowable.

In regard to claim 7, the Examiner states that Watt teaches an MOS with a gate applied with a bias voltage. The Examiner is requested to point out in the reference where this feature is shown. Likewise, in claim 8, the second bias voltage is gated. The Examiner is also requested to point out where in the reference this limitation appears.

In regard to claims 9 and 10, the Examiner agrees that the Watt reference does not show this arrangement of the wells. However, the Examiner feels that it would have been obvious to do so to provide better device isolation. Applicants submit that this would not be obvious since there is no teaching in the reference of the need to do so and no indication that such isolation is necessary. Accordingly, Applicants submit that these claims are additionally allowable.

Likewise, Applicants submit that claims 11, 12, and 15 are also allowable as presenting additional limitations not seen in the references.

Conclusion

In view of the above remarks, it is believed that the claims clearly distinguish over the patents relied on by the Examiner, either alone or in combination. In view of this, reconsideration of the rejection, and allowance of all the claims are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment(s)